Reference-less, real time on-chip Clock Jitter measurement IP

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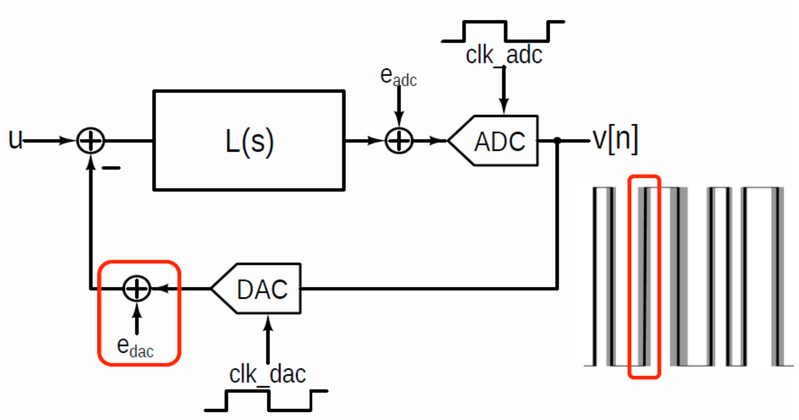
Introduction

Abstract

A novel IP is presented for on-chip clock jitter measurement scheme without the need of any reference entities. The proposed technique utilizes the degrading effect of jitter on performance metrics of a Continuous Time Sigma Delta Modulator based Analog to Digital Converter (CTSD ADC). The impact of jitter on modulator performance is very systematic and quantifiable. This coherent jitter influence on SNR (Signal to Noise Ratio) of the CTSD ADC is deployed into an architecture for in-situ jitter measurement during the operational, test or debug phase. The output response is analyzed on-chip using a simplified version of the sine-wave fitting algorithm to compute the SNR. The achieved performance is scalable with technology node and can in principle be increased as much as desired. High measurement resolutions less than 1pS can be achieved.

Impact of Clock Jitter on a Delta Sigma Modulator

- Additive error following the DAC => $e2(t)$ depends on DAC properties.
- Equivalent to adding an error at the modulator input.
- Degrades performance. Merits careful analysis.



Jittery clock → equivalent to error at the input

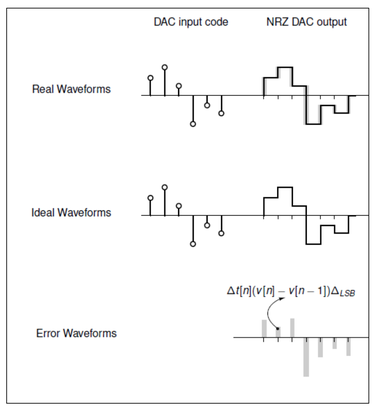
Effect of Clock Jitter on NRZ DACs

$$\varepsilon(n) = (y(n) - y(n-1))\frac{\Delta T(n)}{T_s}$$

The in-band Signal to noise ratio due to jitter

$$SNR_j = \frac{A^2/2}{B_w \cdot (\sigma_{\Delta T})^2 \cdot \left[\frac{A^2\omega_i^2}{f_s} + \frac{X_{FS}^2 \cdot f_s}{3}\right]}$$

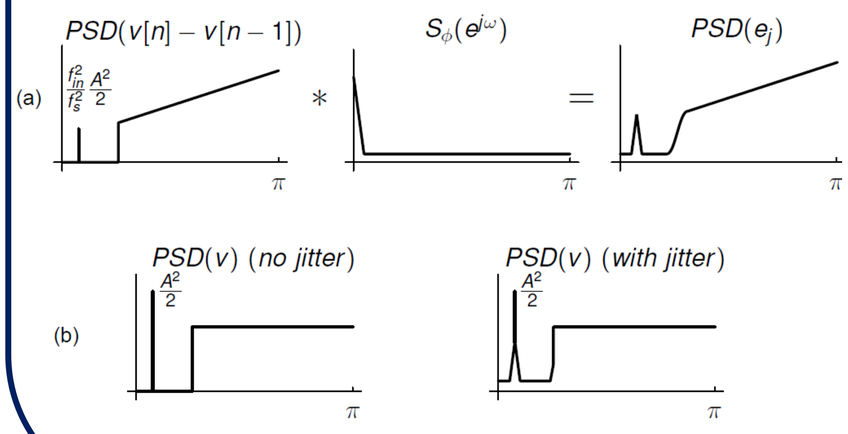
A - signal amplitude, ω_i - angular freq.
B_w - bandwidth
and $\sigma_{\Delta T}$ is clock jitter standard deviation of the modulator clock



Ref: "Effect of Clock Jitter Error on the Performance degradation of Multi-bit Continuous-Time ΣΔ Modulators With NRZ DAC", TEC2004-01752/MIC January 2005.

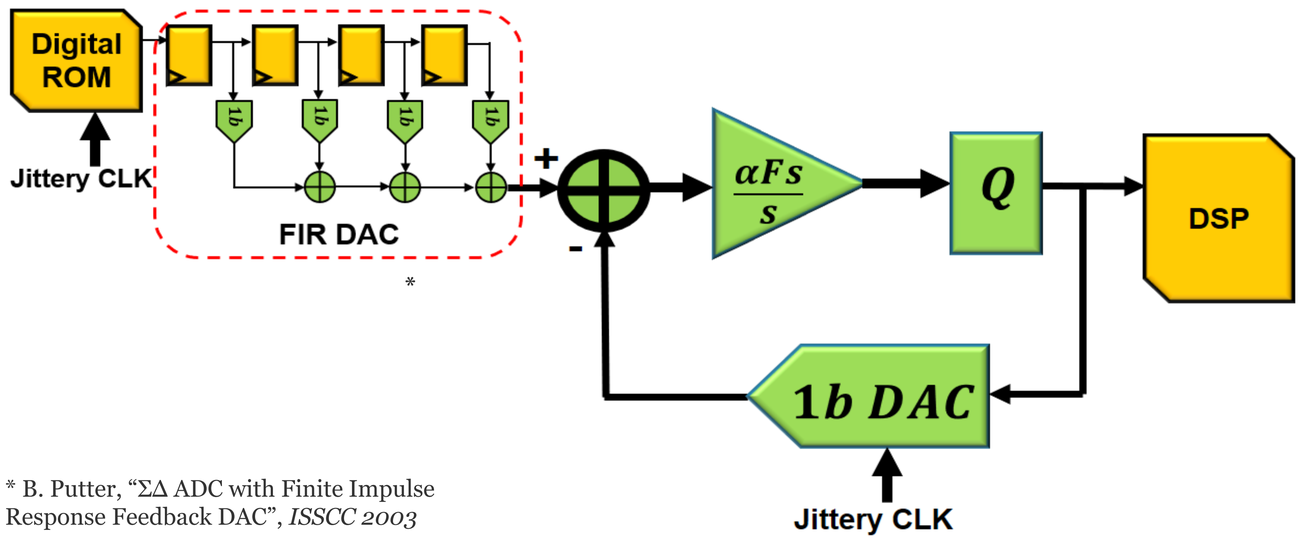
Real Clocks and Phase Noise

$$e_j[n] = (v[n] - v[n-1])(\Delta t[n]/T_s)$$

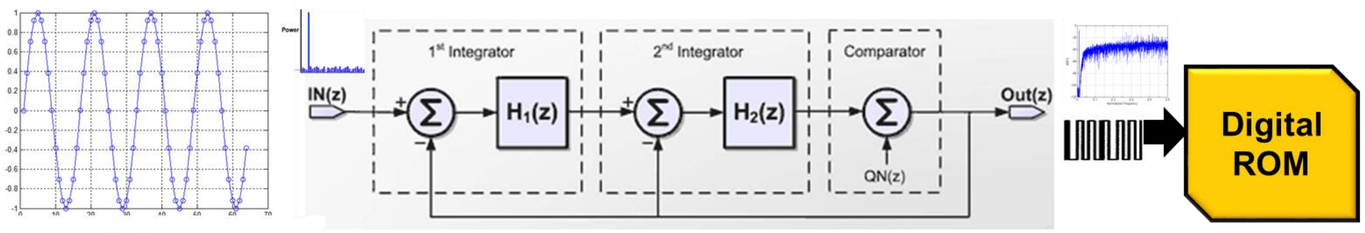


Novel Architecture

Novel Jitter measurement IP

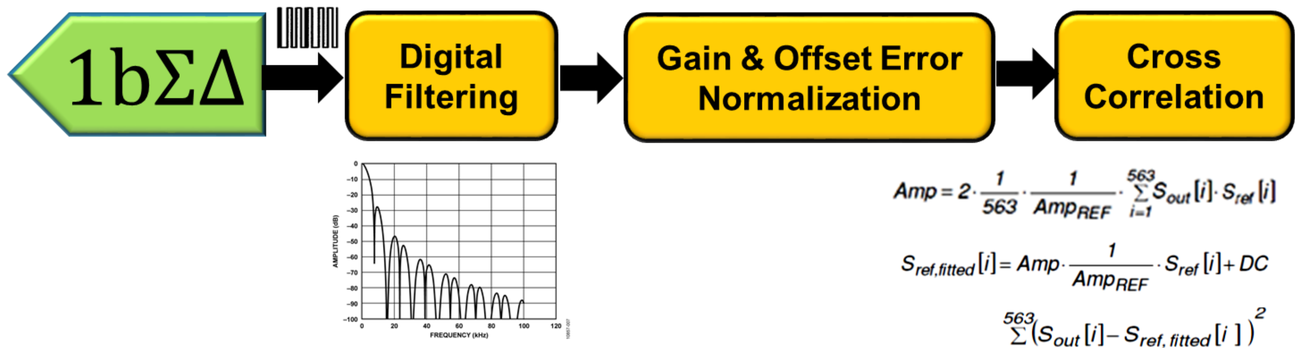


* B. Putter, "ΣΔ ADC with Finite Impulse Response Feedback DAC", *ISSCC 2003*



$$X_k = \sum_{n=0}^{N-1} x_n \cdot e^{-\frac{2\pi i}{N} kn}$$

Digital Higher Order Modulator



$$Amp = 2 \cdot \frac{1}{563} \cdot \frac{1}{Amp_{REF}} \cdot \sum_{i=1}^{563} S_{out}[i] \cdot S_{ref}[i]$$

$$S_{ref,fitted}[i] = Amp \cdot \frac{1}{Amp_{REF}} \cdot S_{ref}[i] + DC$$

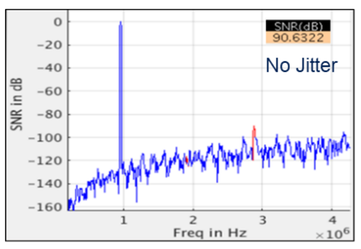
$$P_{error} = \frac{\sum_{i=1}^{563} (S_{out}[i] - S_{ref,fitted}[i])^2}{563}$$

Ref: A Fully-Digital BIST Wrapper Based on Ternary Test Stimuli for the Dynamic Test of a 40 nm CMOS 18-bit Stereo Audio CTSD-ADC, IEEE Transactions on Circuits and Systems I, Oct. 2016

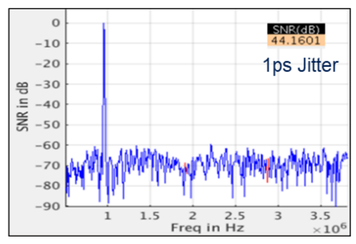
Results & Conclusion

Influence of clock jitter on a continuous time (CT) sigma-delta ADC:

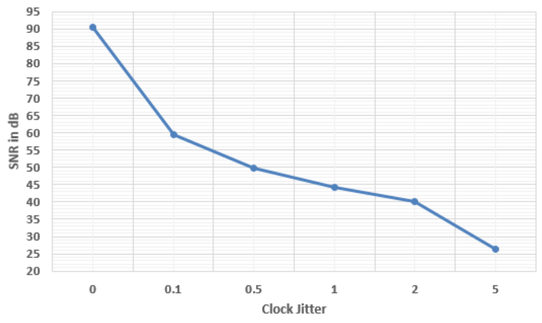
- Illustration of in band frequency spectrum with the system clock subject to jitter degradation.
- High measurement resolution less than 1pS is achieved.



(a) Reference Spectra



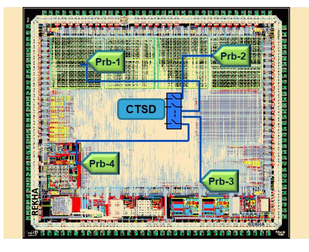
(b) Spectrum for 1ps Jitter

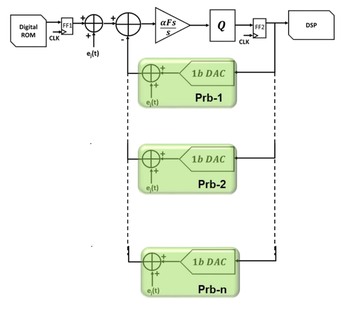


(c) SNR degradation for a 960 KHz sinusoid

Key Benefits:

- Fully on chip solution
- Obviates need of any reference clock or PLL
- Can help SoC architect as a jitter sensor and thus reduce design margins (SoC PPA improvement)
- High resolution quantification of rms jitter
- Immune to PVT variations
- Multi probe solution leads to low area overhead





SoC solution using multiple remote probes across chip